Estimating the Design Value(s) Of the Shunt-Peaking Inductor(s) in CMOS Trans-Impedance Amplifier System by Placement of Poles and Zeros

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***Abstract*— This article provides a guideline towards estimating the design value(s) of the shunt-peaking inductor(s) used in a wide-band CMOS amplifier system. Mathematical analysis and numerical technique followed by circuit simulation, have been used to demonstrate the feasibility of the approach. The procedure applied to a common-gate amplifier in 0.5 micron CMOS technology produces a simulation result with 51.8 dBΩ gain, 4.32 GHz bandwidth, a peaking < 1dB, with 2.8 mW of DC power. Similarly, the design of an interstage PI configuration of inductors, demonstrates a -3dB bandwidth of 37 GHz, peaking <0.3 dB with a total inductance of 2.24 nH.**

I. INTRODUCTION

A trans-impedance amplifier is an important subsystem in the modern day optical communication system [1]. The amplifier is required to have a very wide bandwidth [2]. In the recent past, researchers have introduced integrated inductors [3],[4] to widen the bandwidth to GHz range. While single and multiple inductors have been used to broaden the band-width, a clear picture for obtaining the range of prospective inductance values supported by adequate mathematical analysis with the aim of bandwidth widening, seems to be lacking in the open literature [5]-[7]. The present article is an attempt to address this void.

To achieve this goal, a combination of analytical and numerical (MATLAB) technique followed by circuit simulations (pSPICE, level=3), have been proposed in this article. The technique has been demonstrated by (i) using the layout data of common-gate (CG) amplifier in a 0.5 micron CMOS technology [4], and (ii) using a an inter-stage PI configuration of inductors [8] with specified capacitive loadings at the input and output. Section II of the article presents the analytical results and the design equations for the range of inductor values to achieve band-width enhancement. In section III the design guidelines derived in section II are applied to two specific cases, i.e., (i) a CMOS CG amplifier, and (ii) an inter-stage PI configuration of inductors. The calculated (using MATLAB) inductance values are applied to verify (using pSPICE simulations) the achievable -3dB bandwidths for the two cases studied. Section IV concludes the article.

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II. ANALYTICAL RESULTS

A. Design of peaking inductor (L) in the basic shunt-peaking circuit:

Fig. 1 presents the basic circuit which has an impedance function given by

$$T_1(s) = \frac{v_o}{i_s'} = R\frac{\omega_o(s+\frac{\omega_o}{m})}{s^2 + s\frac{\omega_o}{m} + \frac{\omega_o{}^2}{m}} \quad (1)$$

where, $\omega_0 = 1/CR, m = \omega_z/\omega_0$ and $\omega_z = R/L$

Peaking occurs for complex poles of $T_1(s)$ and this happens when $L>0.25CR^2$. Further, the condition that the pole frequency $\omega_C=1/\sqrt{(LC)}$ of the system should be greater than the RC time- constant frequency ω_o for band-width extension, leads to $L<CR^2$. The guideline for the design of the inductance thus becomes $0.25CR^2<L<CR^2$. In Fig. 2(a) shows that with m=0.7, i.e., L_{opt} =$0.7CR^2$ an optimum bandwidth expansion ratio (i.e., $BWER$= ω_{3dB}/ω_o) of 1.85 can be achieved [9]. The peaking remains below 2 dB (Fig. 2(b)).

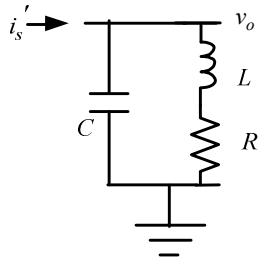
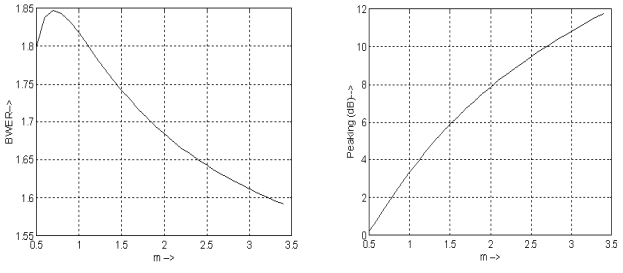


Figure 1: Basic *L, R, C* shunt-peaking circuit.



(a) (b)

Figure 2: (a) *BWER* vs. *m*, (b) Peaking (in dB) vs. *m*.

B. Design of peaking inductor (L) in common-gate CMOS amplifier

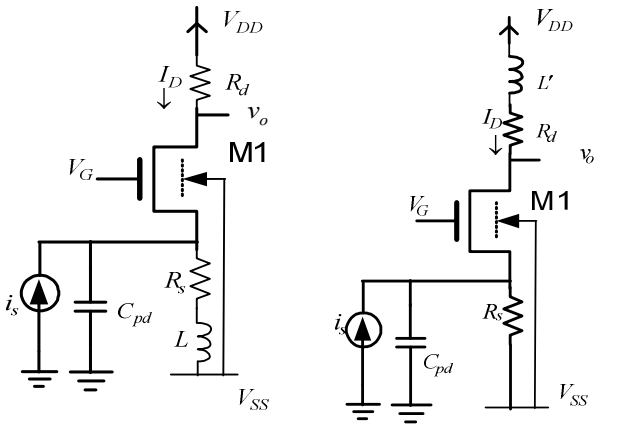


Figure 3: CG amplifier with shunt-peaking inductor (a) at source, (b) at drain of the CMOS amplifier.

Consider Fig.3(a) which depicts a CMOS common-gate (CG) amplifier. The input is a photodiode current source with its parasitic capacitance C_{pd}. The shunt-peaking inductor L is placed in series with the resistance at the source. The transimpedance function is given by

$$T_1(s) = \frac{v_o}{i_s} = \frac{(g_m + g_{mb})(1 + sLg_S)}{a_3 s^3 + a_2 s^2 + a_1 s + a_o} \tag{2}$$

The coefficients a_o, a_1, .. depend upon the *ac* equivalent circuit parameters of the MOS transistor. g_m is the gate transconductance, g_{mb} is the body transconductance of the transistor. Further, g_d=1/R_d, g_S =1/R_S, C_1=C_{pd}+C_{gs}+C_{bs}, C_2= C_{gd}+C_{db}, and a_o=g_d(g_m+g_{mb}+g_S), a_3=$C_1C_2Lg_S$. In absence of the inductor L, the system becomes of order two with a bandwidth approximately equal to the dominant-pole frequency [10]

$$\omega_d = \frac{g_m g_d + g_d g_s + g_{mb} g_d}{g_m C_2 + g_{mb} C_2 + g_s C_2 + g_d C_1} \tag{3}$$

The band-edge frequency (BEF) of the system is Ω_B=$(a_o/a_3)^{1/3}$, with the zero at ω_Z =1/Lg_s For bandwidth expansion relative to ω_d we will interleave ω_z in between ω_d and Ω_B, i.e., $\omega_d < \omega_z < \Omega_B$. According to the principles of Bode plot interleaved placement of poles and zeros will result in a magnitude plot where the slopes due to the poles and zeros will tend to cancel each other, thereby producing a maximally flat magnitude response (or response with small ripples) over an wider range of frequencies. That will bring in a wide bandwidth of operation. Application of the above principle leads to the range of designable inductance as:

$$R_s^{3/2}\left(\frac{C_1 C_2 R_d}{a_o}\right)^{1/2} < L < \frac{R_s}{\omega_d} \tag{4}$$

The actual value of L can be chosen from the range of indicated by (4) together with any system specification regarding the bandwidth expansion (relative to ω_d) required against the amount of peaking that is acceptable. The shunt-peaking inductor L' could also be positioned at the drain of the common-gate stage, as shown in Fig. 3(b). In this we can similarly derive the design inductance to be in the range (with ω_z'=R_d/L', Ω_B'= $= (a_o'/a_3')^{\frac{1}{3}}$, and assuming r_o as infinity),

$$R_d^{3/2}\left(\frac{C_1 C_2 R_s}{a_o'}\right)^{1/2} < L' < \frac{R_d}{\omega_d} \tag{5}$$

In the above, $a_o' = g_d(g_m + g_{mb} + g_s)$, and $a_3' = C_1 C_2 L' g_d$, g_d=1/R_d.

C. Design of peaking inductor (L) in an inter-stage coupling network

Consider Fig.4 which shows an inter-stage coupling network between two amplifier stages. This consist of two L,C,R resonant circuits connected via a floating inductor L_C. C_{p1} is the parasitic capacitance at the output of the preceding amplifier while C_{p2} is the parasitic capacitance at the input of the following amplifier. The inductors are arranged like a PI symbol and the overall configuration can be considered as a PI-peaking (PIP) circuit [8]. The transimpedance gain is given by

$$T_2(s) = \frac{v_o}{i_s'} = \frac{b_2 s^2 + b_1 s + b_o}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_o} \tag{6}$$

The coefficients in (6) that influence the bandwidth are given as:

$$\begin{aligned} &g_{d1} = 1/R_{d1},\ g_{d2} = 1/R_{d2},\ g_o = 0 \text{(assumed)} \\ &a_o = g_{d1} + g_{d2} \\ &a_3 = g_{d1}g_{d2}C_{p1}L_C L_1 + g_{d1}g_{d2}C_{p1}L_1 L_2 + C_{p1}C_{p2}L_C \\ &+ g_{d1}g_{d2}C_{p2}L_C L_2 + g_{d1}g_{d2}C_{p2}L_1 L_2 \\ &a_5 = g_{d1}g_{d2}C_{p1}C_{p2}L_C L_1 L_2 \end{aligned} \tag{7}$$

Unfortunately, in [8] detail design guideline has been provided only for a second order system involving one of the three inductors.

Without the PIP elements, the inter-stage parasitic capacitance $C= C_{p1}+C_{p2}$ could be tuned off with a series *L, R* circuit as in Fig.1. It is interesting to investigate the possibility to exploit the use of the PIP structure to obtain a $BWER= N >M =1.85$ with a total inductance $L_{tot} =L_1+L_2+L_C \leq ML_{opt}$, where $L_{opt}= m_{opt}CR^2$, with $m_{opt} =0.7$. Towards this, let $R_{d1}=R_{d2}=2R$, and let the reference time-constant frequency be $\omega_o=1/(2R_{d1}C_{p1})$ as used in [8]. Let $L_1=m_1(2R)^2C_{p1}$, $L_2=m_2(2R)^2C_{p2}$, $n=C_{p2}/C_{p1}$. In absence of L_C, the transfer function becomes of order three with the BEF given by $\omega_{B3}^3 =a_o/a_{3X}$ where $a_{3X}=g_{d1}g_{d2}C_{p1}L_1L_2+ g_{d1}g_{d2}C_{p2}L_1L_2$.

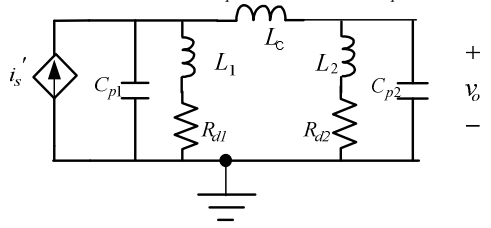


Figure 4: The PI configuration of inductors for band-width extension

We will attempt to arrange $\omega_{B3} > \omega_{B2}$, where ω_{B2} is the BEF of the optimized series *L, R* peaking circuit, i.e., $\omega_{B2} =1/\sqrt{(L_{opt}C)} = \omega_o/\sqrt{(m_{opt})}$. Since ω_{B2} is > ω_o (the *RC* time-constant frequency), our choice will lead to a higher possible overall bandwidth of the system. We can then derive

$$m_1 m_2 < \frac{(n+1)^2}{4n}(m_{opt})^{3/2} \tag{8}$$

Actual value of *n* should be ascertained from the extracted layout data for the system.

On inserting L_C, the transfer function becomes of order five, as in (6), with the new band-edge frequency given by $\omega_{B5} =(a_o/a_5)^{1/5}$. This can be expressed as

$$\omega_{B5}^5 = \frac{\omega_{z1}C_{p2}\omega_{p2}^2 + \omega_{z2}C_{p1}\omega_{p1}^2}{C_{p1}C_{p2}L_C}, \text{ with } \omega_{z1} = 2R/L_1,$$
$$\omega_{p2}^2 = 1/L_2C_{p2}, \omega_{z2} = 2R/L_2, \omega_{p1}^2 = 1/L_1C_{p1} \tag{9}$$

If $n>1$ we will position $\omega_{z2} < \omega_{B5} < \omega_{z1}$, leading to the design range for L_C as:

$$\frac{8R^2m_1^4C_{p1}}{n^2m_2} < L_C < \frac{8R^2n^3m_2^4C_{p1}}{m_1} \tag{10}$$

If n<1, we will place $\omega_{z2} > \omega_{B5} > \omega_{z1}$ thereby giving the designable L_C range as:

$$\frac{8R^2m_1^4C_{p1}}{n^2m_2} > L_C > \frac{8R^2n^3m_2^4C_{p1}}{m_1} \tag{11}$$

III. RESULTS USING MATLAB AND SPICE

A. CG-MOS Transimpedance amplifier with band-width widening

The design guideline in (4) has been verified by using the ac equivalent circuit parameters (g_m=1.45 mS, g_{mb}=0.42 mS) of an NMOS transistor (*width*=25 microns, *length*=2 microns) in a standard 0.5 micron CMOS technology. Using R_S =200Ω, R_d =1500Ω, C_{pd}=250 fF [4] , and the parasitic capacitance data (C_{gs}=8.34 fF, C_{sb} =30.8 fF=C_{db}, C_{gd}=8.17 fF) extracted from the transistor layout, we get (using MATLAB code) the design inductance range as 9.92 nH< *L*< 20.1 nH. Employing *L*=10 nH in the circuit of Fig. 3(a), pSPICE simulation (level=3 for MOS transistors) produces a transimpedance gain of 51.8 dBΩ, and a -3dB bandwidth of 4.32 GHz with a peaking < 1dB. The power consumption from ±1.5 V DC supplies with I_{DC}= 0.92 mA gives the GBW/P_{DC} metric of 608.94 GHz Ω/mW, which is higher than that (~212.12 GHz Ω/mW) reported in [4]. Thus the results reported in this article and the suggested procedure to choose the inductance values could provide a superior design metric value.

B. Interstage inductors for bandwidth widening

The design procedure suggested through (9)-(11) has been pursued with C_{p1}=25 fF, C_{p2}=75 fF which are assumed as typical inter-stage parasitic capacitances in a MOS amplifier system. Thus we have $n = C_{p2}/C_{p1}$ =3. We further used $R_{d1}=R_{d2}$=200 Ω [8]. Thus the *RC* ($C=C_{p1}+C_{p2}$=100 fF, $R=R_{d1}||R_{d2}$=100 Ω) time-constant bandwidth for the circuit on hand is ($f_o=\omega_o/2\pi$) 15.92 GHz.

A MATLAB code has been used to derive several pair of m_1, m_2 values which satisfy the inequality in (8). Few sample values are presented in Table 1. The range of m_1, m_2 values are chosen to demonstrate that our method leads to the range of L_1, L_2, and L_C values that have been used in [8] with successful outcome. PSpice simulations with several choices of L_C -values in the range depicted in Table I produce the bandwidth and (peak-to-peak) ripple values as shown in Table II. It is observed that a bandwidth of up to 39 GHz can be achieved with a ripple of less than 2 dB and a total inductance of less than 5 nH. The bandwidth extension factor in this case is 39/15.91=2.45. Similarly, a bandwidth of 37 GHz can be achieved with a ripple less than 0.3 dB, and a total inductance of 2.24 nH.

In a practical integrated circuit environment, one can adopt the suggested technique by

(i) Extracting the layout capacitors at the interstage and determining the value of *n*.

(ii) Running a MATLAB program to arrive at a set of values of m_1, m_2 pair satisfying (8), and associated L_1, L_2, and range of L_C values.

(iii) Selecting several sets of the inductor values from step (ii) and simulating the responses to narrow down the choice to the values which meet or exceed the system level specifications.

(iv) Laying out the inductors and extracting the broadband *RLC* model for the inductors using, for example, Virtuoso Passive Component Modeler (VPCM) of Cadence system.

(v) Using the extracted values in step (i) and repeating the sequence (ii) to (iv) until an acceptable result satisfying the system level specification is achieved.

It may be mentioned that the above results present the potential bandwidths that can be obtained in the interstage circuit by adopting the procedure suggested in this article.

The actual bandwidth obtained will be further influenced by the transition frequency of the MOS transistor stages, which in turn depends on the DC current drive that can be used with the transistors. This latter factor depends on the transistor sizes (~ substrate area) that can be used, and the power budget at the system level.

TABLE I: A TYPICAL RANGE OF L_1, L_2, AND L_C VALUES

m_1	m_2	L_1 (nH)	L_2(nH)	L_C>(nH)	L_C<(nH)
0.88	0.32	0.88	0.96	0.036	0.64
1.5	0.5	1.5	1.5	0.56	2.25

TABLE II: -3DB BANDWIDTHS AND RIPPLE FOR SEVERAL VALUES OF L_C

L_1	L_2	L_C	f_{3dB}	Ripple
0.88 nH	0.96 nH	0.05 nH	28.7 GHz	0.1 dB
		0.1 nH	29.3 GHz	0.12 dB
		0.4 nH	36.9 GHz	0.26 dB
		0.6 nH	60 GHz	6.52 dB
1.5 nH	1.5 nH	0.6 nH	60 GHz	11.3 dB
		1.0 nH	50 GHz	6.7 dB
		1.6 nH	43 GHz	3.3 dB
		2.0 nH	39 GHz	1.7 dB

C. *Practical considerations regarding the calculated inductors*

In sub-section *B* above, the numerical values of the inductors have been used to predict the expected bandwidth of operation assuming the inductors as ideal. Actual layout of inductors has parasitic components which limit the operating bandwidth of the inductors. From the results reported in [11] it appears that the inductor values of 0.5 nH to 2 nH will have very small parasitic values so as not to invalidate the calculations made above. Further, use of stacked structure [12] and use of special de-embedding structure [13] promise realizability of integrated inductors as low as 0.2 nH with predictable behaviour up to about 100 GHz. Moreover, inductors in the range of 0.2 nH to 1.6 nH have been implemented in a practical 0.18 µm CMOS process with successful outcome [8]. Hence the values calculated using the procedure suggested in this article seems to bear promise for practical and successful implementation.

IV. CONCLUSION

A technique to design the inductance values in a shunt-peaked trans-impedance amplifier system is proposed. We employed a combination of analytical work and numerical simulations to derive a set of designable values for the inductance(s). The concept of band-edge frequency has been used for this purpose since simple analytical calculation of the -3dB frequency is not possible when the order of the transfer function becomes higher than two. The results of analysis and numerical simulation have been used to demonstrate the implementation of very wide band trans-impedance functions with (i) a CG-CMOS amplifier, and (ii) an interstage coupling circuit with three inductors in PI configuration. The design approach proposed in this article could afford to superior performance metrics related to overall power consumption and inductance related substrate area requirement. The results reported in this article are not exhaustive by any measure. These can be considered as demonstration of the principle of interleaved positioning of the pole-zero pairs of the transfer function. More optimum results could be arrived at by careful choice of the m_1, m_2 parameters in Table I. Further work including both the desired band-width and ripple value specifications, to obtain the designable inductor values will be pursued in the near future.

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